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February 22, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 10/020,754 12/12/01

Brian Lee

NEW BURIED STRAP FORMATION METHOD FOR SUB-150 NM BEST DRAM DEVICES

Grp. Art Unit: 1765

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 27, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B Ackerman 2/27/02

U.S. Patent 6,211,006 to Tsai et al., "Method of Forming a Trench-Type Capacitor," discloses a trench-type capacitor.

U.S. Patent 6,124,206 to Flietner et al., "Reduced Pad Erosion," teaches forming deep trench capacitors.

U.S. Patent 6,080,618 to Bergner et al., "Controllability of a Buried Device Layer," discloses formation of a buried strap with little thickness variation. The buried strap is formed where the collar is partially removed.

U.S. Patent 6,008,104 to Schrems, "Method of Fabricating a Trench Capacitor with a Deposited Isolation Collar," discloses a BEST DRAM process.

U.S. Patent 5,981,332 to Mandelman et al., "Reduced Parasitic Leakage in Semiconductor Devices," discloses a BEST DRAM process.

U.S. Patent 6,204,112 to Chakravarti et al., "Process for Forming a High Density Semiconductor Device," reveals memory cell with buried straps and self alligned DT capacitors.

U.S. Patent 6,140,673 to Kohyama, "Semiconductor Memory Device and Fabricating Method," discloses a BEST DRAM process.

U.S. Patent 6,291,286 to Hsiao, "Two-Step Strap Implantation of Making Deep Trench Capacitors for DRAM Cells," reveals memory cell with buried straps and self aligned DT capacitors and HSG.

U.S. Patent 6,284,593 to Mandelman et al., "Method for Shallow Trench Isolated, Contacted Well, Vertical MOSFET DRAM," discloses a buried strap process.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761